Swappable Container Waterborne Transport Battery

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Reducing the Cost of Large Batteries for Waterborne Transport

D4.2

Smart Cell EMC Compatibility

23 December 2024

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CONTENTS

GLOSSARY OF TERMS

Term	Definition
BCU	Battery Controller Unit
BMS	Battery Management System
EMC	Electromagnetic compatibility
MCU	Master Control Unit
PCB	Printed Circuit Board
SCS	Smart Cell Supervisor
SCU	String Controller Unit

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0.3	14-Nov-2024	Small additions to Version 0.2

1.0	16-Dec-2024	Revised Executive and Project summary; revised Partner involvement

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PROJECT SUMMARY

The transport sector contributes to almost a quarter of Europe's greenhouse gas (GHG) emissions. Compared to other sectors, such as agriculture or energy industries, it is the only sector with emissions higher than that of 1990. Waterborne transport emissions represent around 13% of the overall EU greenhouse gas emissions from the transport sector. Moreover, waterborne transport emissions could increase between 50% and 250% by 2050 under a businessas-usual scenario, undermining the objectives of the Paris agreement. The challenge for a large-scale adoption and implementation of batteries for waterborne transport is mainly related to the high costs of the battery systems and cells.

The Current Direct project addresses these challenges by proposing an innovative lithium-ion cell optimized for waterborne transport, using novel manufacturing techniques allowing for a consistent cost reduction compared to the current market prices. Additionally, a swappable containerized energy storage system optimized for cost and operation in the waterborne transport industry will be developed. The overarching aim of the Current Direct project is to develop and demonstrate an innovative interchangeable waterborne transport battery system and EaaS Platform in an operational environment at the Port of Amsterdam at TRL7 that facilitates fast charging of vessels, fleet optimization and novel business models. The Current Direct project is dedicated to (i) significantly reduce the total cost of waterborne transport batteries, (ii) cut GHG emissions of the marine transport sector through electrification of vessel fleets, (iii) increase the energy density of waterborne battery cells and (iv) trigger investments for innovation, job and knowledge creation in the European marine transport and battery sector.

The Current Direct EcoSystem is shown in Figure 1.

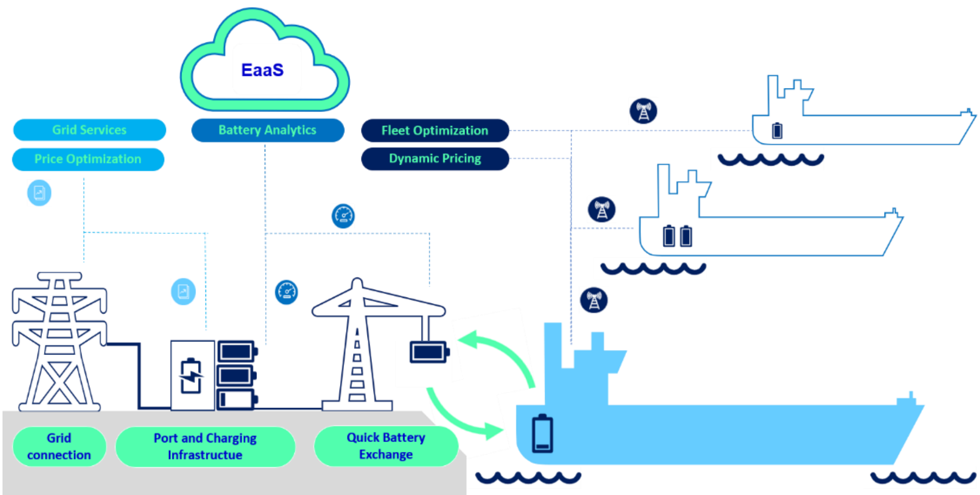

Figure 1. Current Direct EcoSystem

1. EXECUTIVE SUMMARY

The original objective of this report was to verify that the Smart Cell Supervisor (SCS) can communicate without interruption in the full shipboard EMC spectrum. Due to global supply and demand constraints during the COVID-19 pandemic, limiting the availability of the hardware required to develop and construct the SCS components to be subjected to EMC testing, the scope of this deliverable has changed over time. Subsequently, this has led to substantial delay of the submission of this deliverable.

The report describes the development of the SCS starting from the existing VITO BattSense battery management system (BMS) technology (reference solution) and in line with the project's goals and requirements. The reference solution has been subjected to EMC testing which is described in the next section. Based upon those results and the adaptations made within the SCS developments, an estimation is presented for the improvements on EMC performance of the SCS. In a final section an overview is presented on the existing and relevant EMC test standards and a strategy that could be applied on a representative battery system, including the SCS technology. However, due to the aforementioned issues on the global market, the technical capabilities of the testing laboratory at the partners' sites and the technical readiness of the full BMS solution, the project partners haven't succeeded in the execution of that EMC testing.

2. SPECIFIC OBJECTIVES FOR WORK PACKAGE 4

This WP encompasses the design, prototyping, verification testing, and demonstration build of the Current Direct Waterborne Transport Battery optimized for inland and short sea shipping applications. It includes the development of key subsystems that improve safety, reduce cost, improve life, and increase energy density.

Subsystem development began immediately at the start of the project, while the battery design hasn't started until milestone M2 with the requirements was frozen.

Specific Objectives:

- Design a safe, low cost, long life, energy-dense Current Direct Waterborne Transport Battery
- Develop and test ultrasound sensors for determining SOC and SOH
- Develop and test BMS single-cell supervisor
- Develop and test composite structural and thermal plate battery module construction
- Create a thermal model of the battery system to understand heat distribution and dissipation
- Produce prototype Current Direct battery modules
- Test Current Direct battery modules for performance and safety certification
- Design a marine, safety-certified, swappable container for the Current Direct battery
- Integrate and test the Current Direct battery, container, and subsystems

3. INTRODUCTION

The Current Direct maritime application environment presents a unique source of demanding electromagnetic interference and compatibility which is of particular importance when designing a battery system due to the large number of sensors used and their susceptibility to noise and interference.

The identification of applicable EMC standards and a comprehensive test strategy is critical to ensure a successful deployment of the Smart Cell Supervisor, designed for the Current Direct project, in the maritime operating environment.

This report describes the electromagnetic compatibility (EMC) of the proposed battery management system (BMS) as the combination of a Master Control Unit (MCU) and Smart Cell Supervisor (SCS) components that connect to individual battery cells or cell groups (parallel-connected individual battery cells). The proposed complete BMS further comprises multiple String Controller Units and a Battery Controller Unit.

This document introduces the set-up of the BMS with emphasis on the part of the system developed within the Current Direct project and which aimed for improved EMC performance. It then provides some details on the SCS and MCU developments, tailored to the project's goals and requirements. The document further presents the current state of EMC testing and compatibility of the baseline solution based on tests that were performed on VITO's reference SCS solution. Finally, the document provides an overview of relevant EMC test standards and outlines the EMC test plan for the final solution of the MCU + SCS combination.

Smart Cell Supervisor

The proposed Current Direct BMS hardware consists of several components. The Smart Cell Supervisor (SCS) is the lowest level component, and it is closely coupled in a 1:1 relationship to each (set of parallel-connected) single battery cells.

Its design for the application in the Current Direct project is based on VITO's Voltage Balancing Unit (VBU) as both perform similar functions. The SCS is a planned development of the VBU to comply with the project's specifications and requirements as set in Task 2.1. To operate the VBUs, and hence also the SCSs, one master board is needed for multiple VBUs or SCSs. This master board is referred to as BMS Master for the current VITO solution and as Master Control Unit (MCU) for the final Current Direct solution. The current version of the BMS Master and the VBUs are designed for industrial applications and have undergone EMC testing and proven to be compliant within that application.

The SCSs will require an MCU as a driver and gateway to higher-level BMS components, this being the String Controller Units (SCU) and a Battery Controller Unit (BCU). The combination of SCU, BCU, MCU and SCSs will finally have to comply with maritime requirements.

It is understood and acknowledged that there are differences between the existing VBU and the future SCS (and BMS Master and MCU) that are relevant in the context of EMC, see Figure 2 and Figure 3:

1. The waveform linking the MCU to the SCS will be a sine-like wave compared to the historically applied block wave;
2. The SCS is planned to be capable to draw limited power from the battery cells to perform measurements while the MCU is powered down;
3. Components to be added to the SCS to comply with maritime regulations. These components provide redundant overvoltage and overtemperature protection.

These changes have an impact on the EMC performance according to maritime standards.

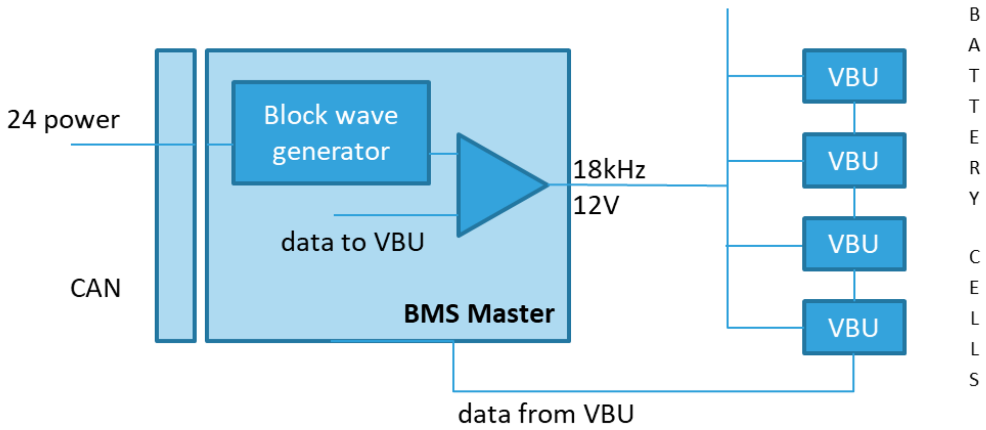

Figure 2 VITO Reference BMS Solution – Hardware Block Diagram

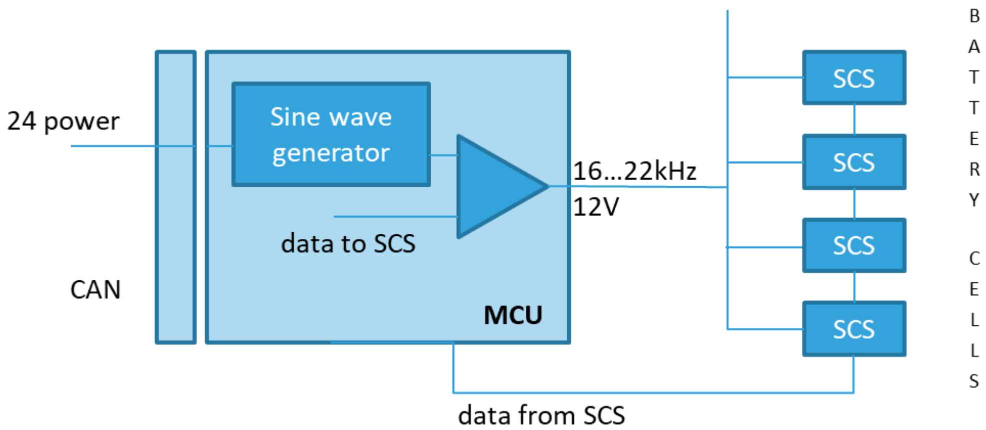

Figure 3 Adapted VITO BMS Solution for the Current Direct Project - Hardware Block Diagram

The main drivers in the SCS and MCU development in the scope of the Current Direct project are:

- Compliance with maritime requirements (set in Task 2.1)
- Compatibility with physical requirements as set by system and sub-system components (e.g. battery cells, modules, ...) (set in Task 2.1)
- Interoperability with BMS components (SCU and BCU)
- Improved resolution and accuracy of voltage measurements
- More frequent voltage measurements
- Full active (and dynamic) cell balancing
- Increasing maximum voltage support per MCU
- Implementation of a battery passport at cell-level

The VITO BMS uses a single line to provide power and data from the master to the VBUs where initially in the baseline solution a 18kHz block wave (Figure 2) is used. To increase the bandwidth this block wave is replaced by a 20kHz sine wave (Figure 3 which results in:

- Higher data rate measured in messages per second,
- Equivalent reliability by adding CRC bits, and
- Uninterrupted power supply while communicating so cell balancing can continue normally while transferring data.

Active cell balancing is performed, so without energy dissipation and in two directions. When a cell needs to be discharged in order to balance it, the energy can be sent back through the inverter towards the MCU's power supply. This power supply is usually not bidirectional so this energy needs to be used by the master and SCS electronics reducing the BMS power consumption. If too many cells need discharge balancing, the excess energy will be sent to cells that need or can use charge balancing. This will always be possible as this only occurs when an important imbalance is required. The RMS value of the balancing current is 190mA. It is shown that communication and balancing can work simultaneously so the communication channel is open permanently greatly improving the average bandwidth compared to the initial design.

The balancing current of the targeted BMS are significantly higher: 400mA in charge and discharge, resulting in a 800mA effective difference between cells.

The maximum sample rate of the BMS has been increased and can be calculated as follows:

Internal data rate = 333 kbps
Number of bits per sample = 18 data + 4 framing
Number of samples per second = 333k / 22 = 15150

Maximum number of cells to sample = 60
System sample rate = 15150 / 60 = 250 or 4 ms per cycle

It is still required to synchronize voltage and current measurements. This is done by the MCU sending a command over the power bus at approximately 20kbps. This introduces a 1ms delay for every cycle, bringing the cycle time to 5ms. It is good practice to limit the bandwidth use to 80-90% in order to account for drift in bitrate. Hence the real maximum sampling capability of the BMS is:

150 samples per channel
60 cells per channel
2 channels per MCU

The voltage measurements in the VITO BMS are not multiplexed. Each SCS measures at the same time converting the cell voltage to a digital value calibrated against its own precision voltage reference. At this point two sources of error can be defined:

1. The voltage reference is not exactly what it is supposed to be, it may have an offset or drift over time or with temperature;
2. The analogue to digital conversion is not accurate, it may have a zero or full-scale offset, it may not be linear in its conversion or may even have missing codes. The resolution may be insufficient to capture required changes.

Two changes were adopted in a new design:

1. A more accurate voltage reference will be introduced resulting in a 5V+/- 2,5mV precision including a 6ppm/°C;
2. A 12bit A/D converter was introduced with oversampling producing a 13bit result.

Due to the worldwide shortage of electronics components, the new BMS hardware was not available for the accuracy tests. Hence detailed accuracy estimation tests were performed with prototype SCS boards using the initial voltage reference combined with the 12bit ADC of the newly developed SCS. This allowed to check the added value of the 12 bit conversion with oversampling and a worst case total accuracy.

The voltage reference used in the test setup is considerably less accurate than the required accuracy but it is very stable so it was decided that in order to reach the requirement, a calibration of the voltage reference would be required and would be possible. Indeed, once a BMS is set up for commissioning, a constant voltage in the order of the cell voltage can be applied to all SCSs simultaneously. This voltage is communicated to the MCU that in turn broadcasts it to the SCSs. Each SCS will measure this value and compare it to the value received from the MCU, so the actual value. This allows each SCS to calculate the actual value of its voltage reference. This value is stored in the SCS's EEPROM for later use. The temperature at which the reference is calibrated is also stored to allow temperature drift corrections. This calibration step can be highly automated and will require approximately one minute of extra time in production as all SCSs are calibrated simultaneously.

	Pre-Current Direct VITO BMS	Post-Current Direct VITO BMS
Resolution	11 bit = 2,5mV	13 bit = 0.61mV
Reference accuracy	5mV	2,5mV
Temperature drift	50ppm/°C	6ppm/°C
Measurement accuracy	5mV + 50ppm/°C	1,23mV

Measurements were taken at 20 levels for the cell voltage with oversampling and 5 levels for the ambient temperature on two SCS boards. After correcting for the reference error, the calibration described in the previous paragraph, the following results were obtained (Table 1 and Table 2).

Table 1 SCS 1 accuracy results

Setting [mV]	V_{err} 0 °C [μV]	V_{err} 10 °C [μV]	V_{err} 20 °C [μV]	V_{err} 30 °C [μV]	V_{err} 40 °C [μV]	V_{err} avg [μV]
0	1081	2300	238	2200	2100	1583.8
250	1520	1372	1372	1833	1833	1586.0
500	969	670	1789	1690	1690	1361.6
750	1823	1574	1984	1835	1835	1810.2
1000	973	1482	1892	1593	1000	1388.0
1250	1241	1500	1300	1660	1560	1452.2
1500	661	872	1181	783	900	879.4
1750	638	699	499	660	1269	753.0
200	107	617	926	1136	1036	764.4
2250	284	206	553	713	713	493.8
2500	496	25	435	446	1056	491.6
2750	237	377	67	106	504	258.2
3000	99	18	328	339	339	224.6
3250	1262	993	174	314	296	607.8
3500	728	508	311	222	222	398.2
3750	546	985	875	206	206	563.6
4000	991	773	1073	754	144	747.0
4250	1209	1040	120	1070	460	779.8
4500	1384	1264	445	734	485	862.4
4750	1525	947	737	467	752	885.6

5000	142	546	273	215	115	258.2

Table 2 SCS 2 accuracy results

Setting [mV]	V_{err} 0 °C [µV]	V_{err} 10 °C [µV]	V_{err} 20 °C [µV]	V_{err} 30 °C [µV]	V_{err} 40 °C [µV]	V_{err} avg [µV]
0	1364	343	2200	243	1489	1127.8
250	238	834	834	786	786	695.6
500	486	286	897	798	798	653.0
750	284	646	646	1008	1619	840.6
1000	297	609	609	920	1020	691.0
1250	11	171	882	1143	1143	670.0
1500	115	327	327	1151	1151	614.2
1750	249	411	311	1185	1185	668.2
2000	273	996	996	497	1108	774.0
2250	108	169	780	231	842	426.0
2500	112	486	736	138	138	322.0
2750	85	671	388	451	351	389.2
3000	598	174	436	350	350	381.6
3250	384	522	11	49	562	305.6
3500	197	484	126	61	450	263.6
3750	556	793	329	93	93	372.8
4000	759	948	437	725	114	596.6
4250	808	535	535	872	361	622.2
4500	721	497	14	238	138	321.6
4750	197	634	487	561	50	385.8
5000	299	786	336	51	151	324.6

It is obvious from these tables that the specified accuracy is difficult to attain in the lower voltage range. This range is never used in the context of Li-ion batteries and their models so the high accuracy is not required. The accuracy is still ample sufficient for safety and protection.

SCS 1 has a voltage reference of 4995mV at room 20°C, SCS 2 has a reference of 5003mV. In both cases the measurements were corrected so this should not explain the differences. Digitization or rounding errors could. However, on the final hardware the voltage references will have a 2,5mV accuracy so further investigation into this issue was not considered relevant.

Considering that the final design will be equipped with a voltage reference having a considerably lower temperature drift than the devices under test, that the required accuracy is of lesser interest in the range of 0..1,5V, and that a calibration step can be added to the production of the BMS without considerable economic impact, we consider this project goal to be reached.

Substantial effort has been put in redesigning the MCU and SCS to fit the stringent physical requirements as set by the project in Task 2.1 and to comply with the requirements for maritime applications. Moreover, the development effort has been hindered by shortages in the market of semiconductor material/electronics during the COVID-19 pandemic. The re-design activities have led to the SCS and MCU designs as can be seen in the following figures.

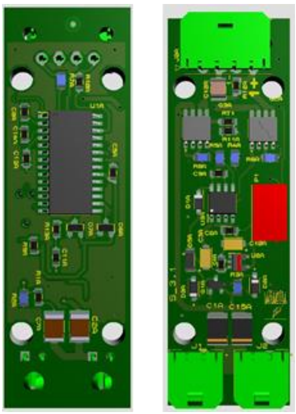

Figure 4 First Smart Cell Supervisor design

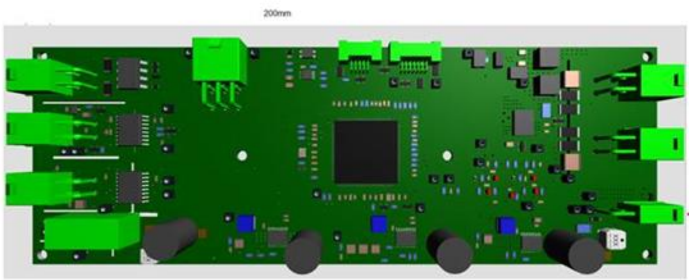

Figure 5 First Master Controller Unit design

Only in Q3 of 2022 a first layout of the SCS Master printed circuit board (PCB) was produced and evaluated.

Testing demonstrated the need for further layout improvement. A second layout version of the SCS master was delivered in Q4 of 2022. This layout version (see Figure 6 and Figure 7) has proven to be stable under all test conditions.

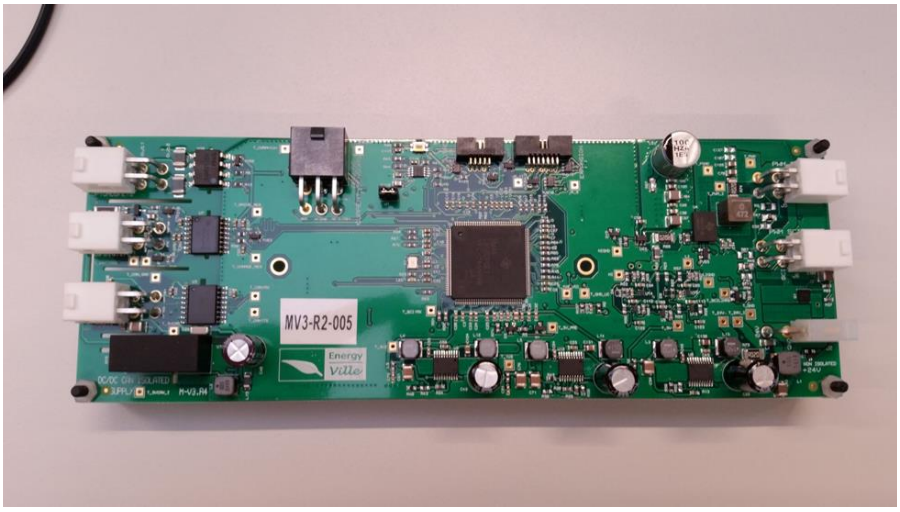

Figure 6 Second revision of the MCU

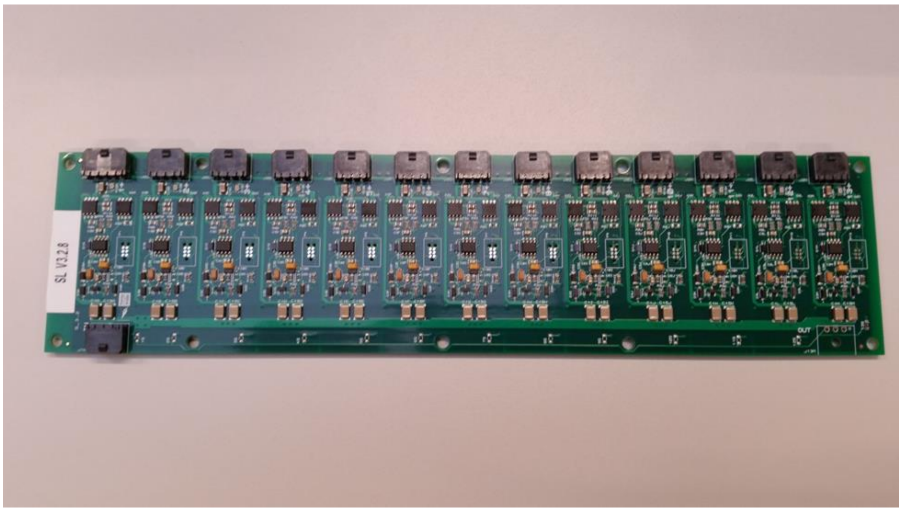

Figure 7 Second revision of the SCS. 13 identical units on one PCB in this hardware for validation testing.

The SCS+MCU combination has undergone intensive testing and provides the requested features:

- Combined power/command bus from MCU to SCSs based on sine wave for improved EMC behavior;
- Cell voltage balancing using active charging and active discharging without resistive losses;
- Increased communication speed from SCSs to MCU @ 333kbps;

- 12 bit accuracy in cell voltage measurements: a calibration setup with software tools has been built to calibrate individual SCSs;
- Cell passport: statistics stored in smart cell local controller (see Figure 8);
- Full BMS functionality as available in reference VITO BattSense BMS technology;
- Firmware upgrade for master over CANbus has been demonstrated;
- VITO has reworked the BattSense SCS communication protocol:
  - CRC error detection
  - Protocol extensions so all new features can be monitored using a PC application.

Figure 8 Representation of cell passport implementation on the SCS.

4. REFERENCE SOLUTION AND EMC TEST RESULTS

This section provides an overview of the reference VITO BMS solution and pre-compliance EMC tests completed and the results generated.

For EMC testing the VITO BMS was assembled and integrated into an industrial-style 14 NMC cell battery with a casing (Figure 9). This system is self-powered in the sense that the BMS draws its power from the battery leaving only the battery terminals and a CAN bus connection exposed to the outside world (Figure 10).

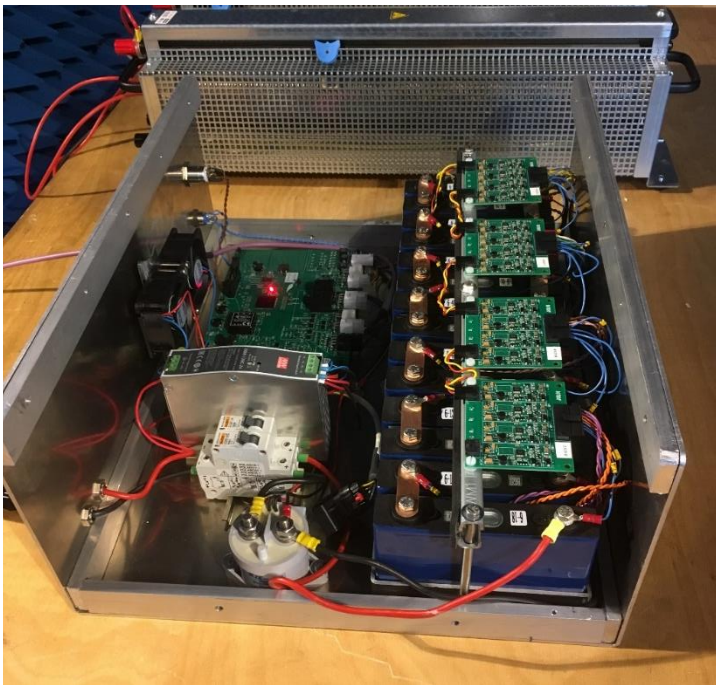

Figure 9 Picture Showing the Inside of the Reference BMS EMC Test Battery

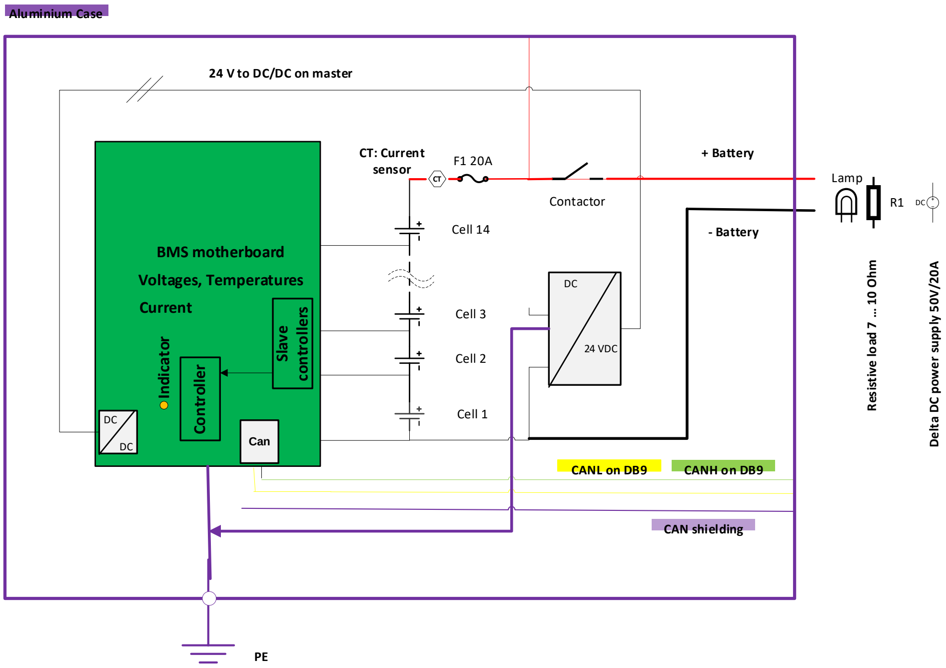

Figure 10 Block Diagram of the Device Under Test

Where a load in the test was required, either wound rheostats or lamps were used. A Delta DC power supply was used as a charger.

An overview of the EMC tests, their related standards, reports, and results are presented in Table 3.

Table 3. EMC Tests, Related Standards, Reports and Results

EMC Test	Standard	Report Reference	Result
Electrostatic discharge Immunity (ESD)	IEC 61000-4-2 Ed. 2.0: 2008 EN 61000-4-2: 2009	30-DS25-CO-200121_1355	PASS
Electrical fast transient/ burst immunity (EFT)	EN 61000-4-4:2012	30-DS25-CO-200121_1355	PASS
Surge immunity	EN 61000-4-5 2006	30-DS25-CO-200121_1355	PASS
Conducted Emissions	EN55022 for class B devices	30-DS25-BMS-VITO-EMC Test 9) p18	PASS [1, 2]
Radiated Emissions	EN55022 for class B devices	30-DS25-BMS-VITO-EMC Test 25) p43	PASS [1,2]
Conducted Immunity	IEC 61000-4-6	30-DS25-BMS-VITO-EMC	PASS
Radiated Immunity	IEC 61000-4-3	30-DS25-BMS-VITO-EMC	PASS

[1] Dedicated measure taken on the original BMS master (MCU) to ensure EMC pre-compliance.
[2] Dedicated measures taken on the battery system to ensure EMC compliance.

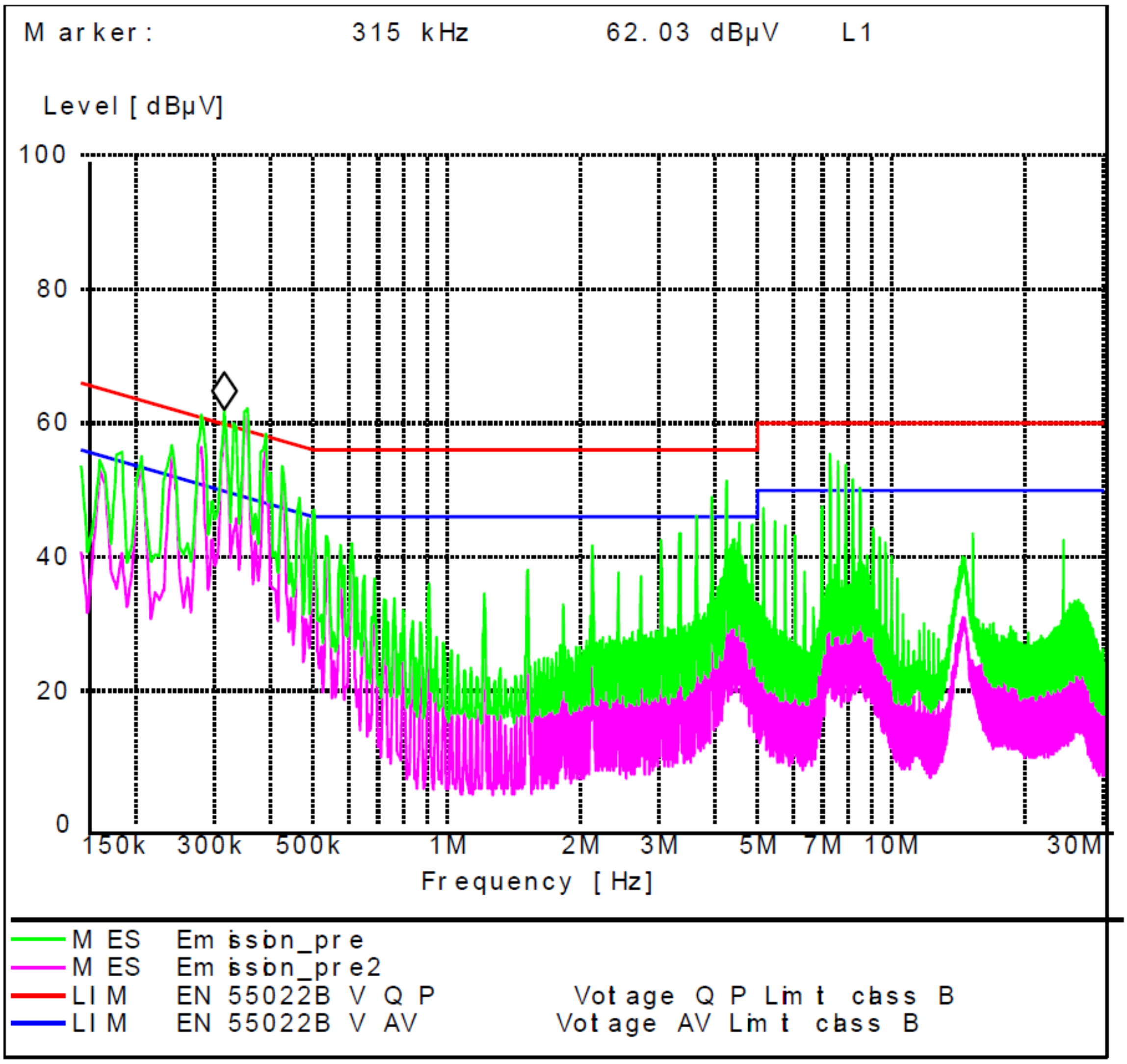

Figure 11 Initial conducted emissions on VITO reference BMS

In the conducted emissions test, the harmonics of the 18 kHz frequency block wave are seen: (165, 205, 240, 275, 315 kHz), see Figure 11. From this figure it can be seen that at first, pre-compliance couldn't be reached. Hence, dedicated measures were taken.

Dedicated measure taken on the original BMS master (MCU) to ensure EMC pre-compliance:

- Replace internal DC/DC converter (CUI/TRACO)
- Minor changes to master PCB power supply circuit (component values)

These measures were determined by an elimination process during EMC testing and were forwarded to the production version.

Dedicated measures taken on the battery system to ensure EMC compliance:

- Remove contactor and fuse, re-laying power wires in the test setup
- 10nF Y cap added (battery + and - to chassis)
- 470nF X2 cap added (battery + to -)

After implementation of the measures above, both the Conducted and Radiated Emissions EMC tests were passed, see Figure 12 and Figure 13.

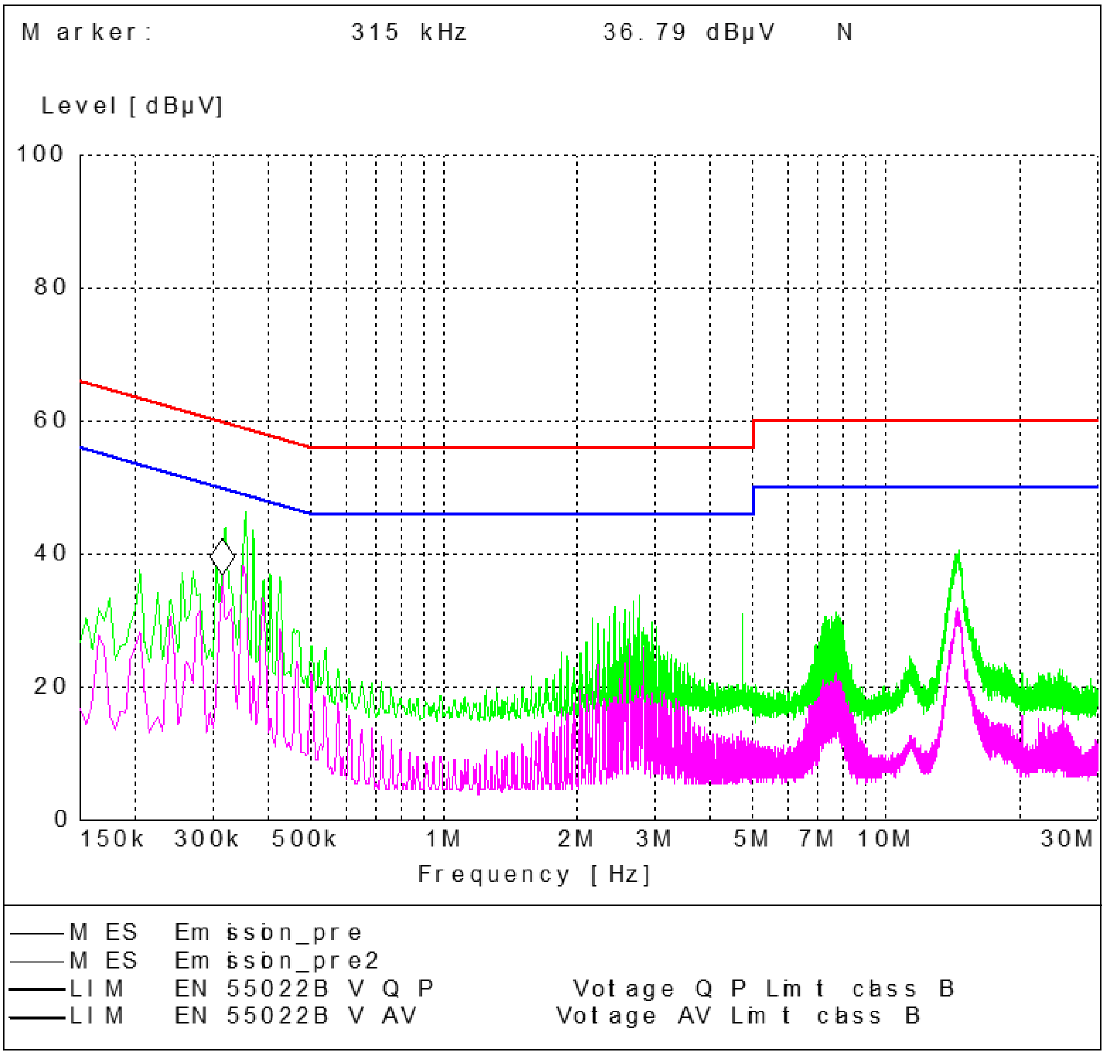

Figure 12 Conducted emissions on VITO reference BMS after dedicated measures

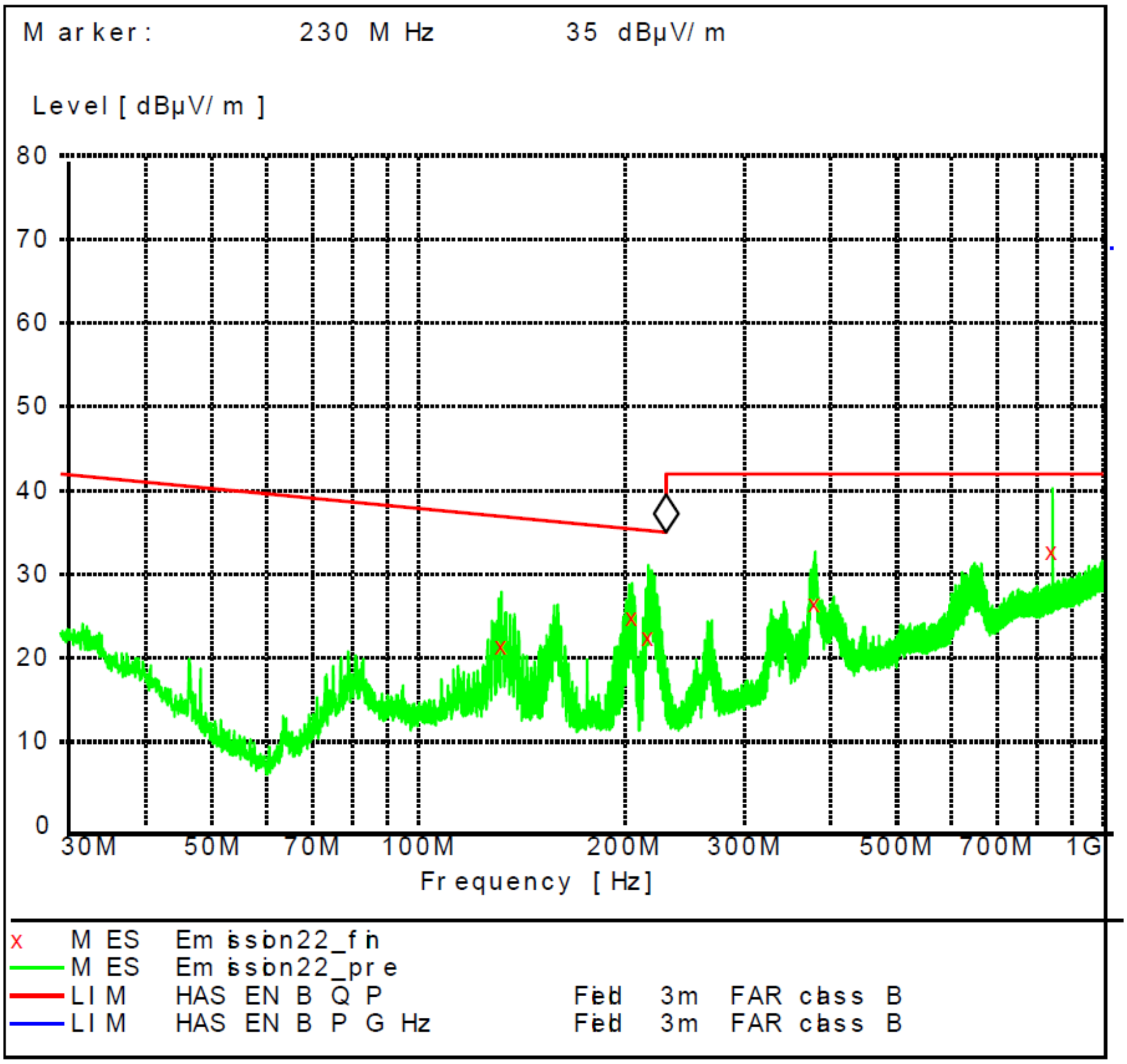

Figure 13 Radiated emissions on VITO reference BMS after dedicated measures

A square (block) wave has steep flanks and this can lead to higher EMC emissions. Therefore in the new design the linking waveform between the MCU and the SCS is a sine-like wave form; it is expected that a sine wave form contributes to a reduction of EMC emission.

For reducing the EMI noise level the following items are included in the new hardware MCU design

- Sine wave form to SCS
- Every DC-DC convertor on the MCU has its own EMI input filter
- Every DC-DC convertor has a light variate switching frequency

The following integration guidelines were found to provide improved EMC performance:

DC Power Cables

- Keep the + and the – of the DC Power Cable short together; avoid loops;

- Avoid loops in DC Power Cable as much as possible;
- Keep the length as short as possible for the DC Power Cables;
- Keep the DC Power Cables as close as possible to a conductive plate.

Signal Cables

- Use twisted pair 0.5 mm² (20AWG) non shielded cable between the slave boards hosting the VBUs (SCSs); maximum parasitic capacitor 200 pF per cable;
- Keep the Signal Cables as far as possible away from the DC Power Cables;
- Keep the Signal Cables as close as possible to a conductive plate;
- If Signal Cables cross the DC Power Cables, do it with a right angle;
- Use shielded twisted pair cable for CANbus communication.

Earthing

- Never combine noisy, "high power" circuit grounds with "low powered" signal circuit grounds;
- Keep high power grounds as short as possible;
- Keep low power grounds together; keep them as short as possible;
- Ensure good conductive contact between metal chassis (earth) and grounding signal.

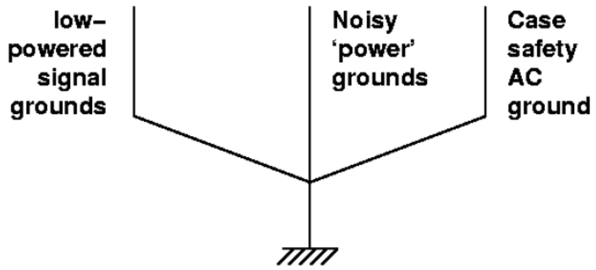

Figure 14 Grounding Guidelines

Enclosure Box

- Ensure good conductive contact between the whole enclosure box (no paint, ….)

5. EMC TEST STANDARDS AND STRATEGY

The maritime application environment presents a source of demanding electromagnetic interference which is of particular importance when designing a battery system due to the large number of sensors used. The identification of applicable standards and a comprehensive test strategy is critical to ensure the successful deployment of Current Direct in the maritime operating environment.

In this section, a comprehensive EMC test strategy is outlined. This test strategy was planned to be applied throughout the development of Current Direct and incorporate all applicable certification standards and tests.

EMC Test Strategy

To manage and mitigate the risk of EMC, validation testing was planned to begin at the component level during Current Direct's development. After subcomponents are validated, testing will then be conducted at the system level. Following this, the Current Direct project results will then be tested to receive EMC certification from the relevant authorities per the identified standards and project requirements as defined under WP2 Specification and Requirements.

5.1.1. EMC Validation Steps Summary

EMC validation can be summarized in three main steps:

1. **EMC Component Tests:** This step aims to validate individual components separately before being integrated into the larger battery system. This step allows the development effort to be de-risked before conducting system-level validation. These tests must represent the real application environment.
2. **EMC System Validation:** This step aims to validate the fully integrated system to ensure fully compatible operation. This ensures that the system will pass all expected criteria before being subjected to certification tests. These tests must represent the real application environment.
3. **EMC Certification:** This step aims to perform the regulatory EMC tests to have the certification from an accredited laboratory.

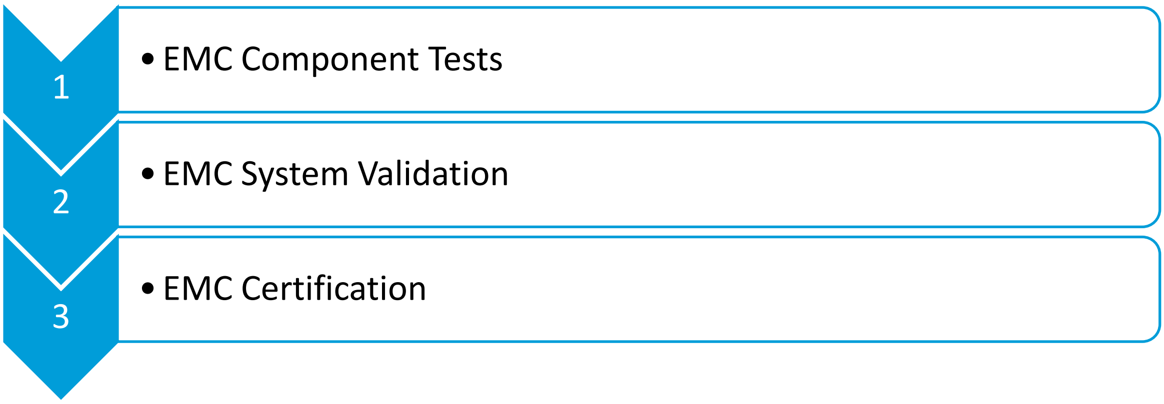

Figure 15 EMC Validation Steps

5.1.2. Test Flow Chart

Validation tests were planned to be conducted with 2 samples in the sequence shown below in Figure 16. If the results are different or there is doubt in performance during characterization, additional tests will be performed on the 3rd sample.

The test laboratory should be organized and run under ISO/IEC 17025. All test equipment used for measuring must be calibrated as per ISO/IEC 17025.

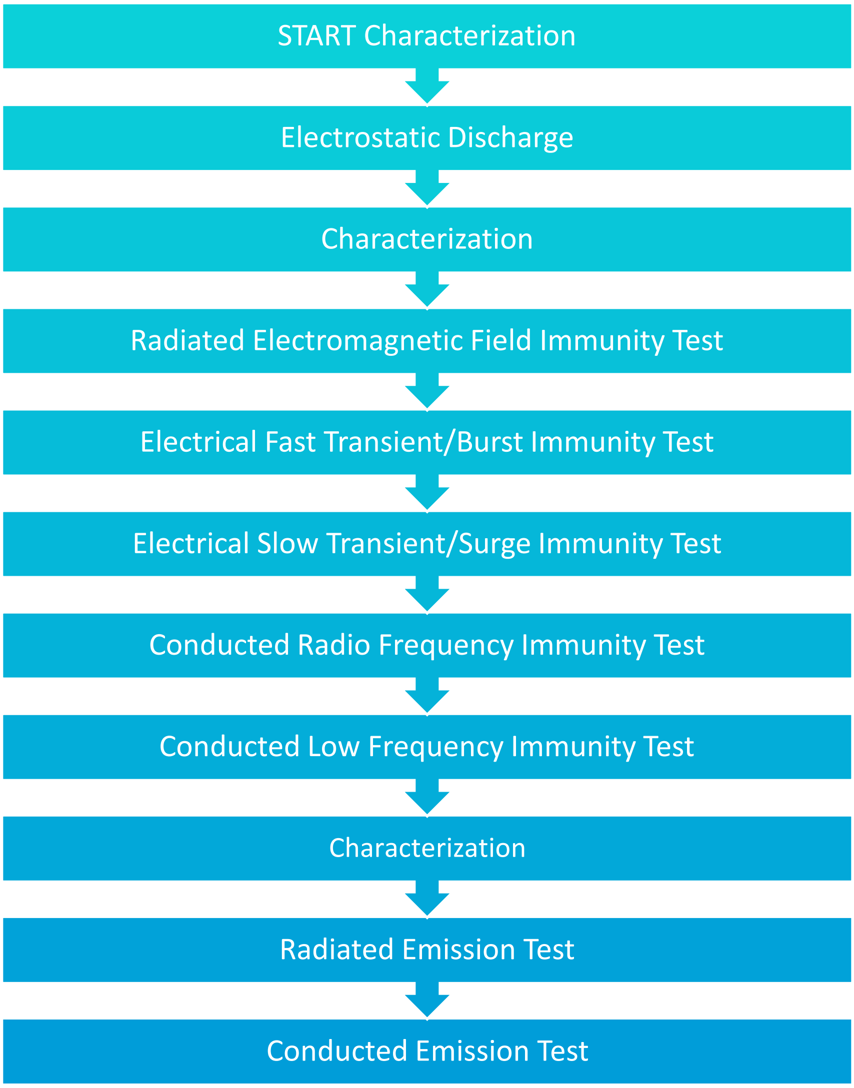

Figure 16 Test Flow Chart

These EMC tests are chosen from the reference standard: DNVGL-CG-0339. The structure was defined to make the most onerous and stressful tests first. The emission tests are conducted at the end of the test sequence to check and confirm whether the immunity test had any effect on the product. The functional characterization will be conducted after the Electrostatic Discharge test and immunity tests to verify acceptable component operation.

Current Direct components will be classified into two categories according to risk levels and the sources of noise. This grouping can be shown below in Table 4.

- Category A: Immunity Risk + No Source of Noise.
- Category B: Immunity Risk + Source of Noise

Table 4 Applicable Tests for Each Category

Tests	Category A	Category B
Emissions	NA	A
Immunity	A	A
ESD	A	A

A: applicable // NA: not applicable // O: Optional (for information only)

Applicable Test Standards

The reference applicable test standards are based on the international maritime standard DNVGL-CG-0339. This standard covers all EMC aspects (ESD, Immunity and Emission). Furthermore, it gives the test levels as well as the acceptance criteria. These standards are used for certification, but their test conditions and acceptance criteria will be made more demanding for both the component and system validation tests to capture the true operating environment conditions.

Table 5 provide the list of applicable standards.

Table 5 List of Applicable Standards

Standard	Description
(IACS) – Unified Requirements	UR E10 – Test Specification for Type Approval
Lloyd's Register Type Approval System – Dec 2020	Test Specification no.1 – Performance and Environmental Test Specification for the following Environmentally Tested Products used in Marine Applications: Electrical Equipment, Control and Monitoring Equipment, Instrumentation and Internal Communication Equipment, Programmable Electronic Systems
DNVGL-CG-0339:2019	Environmental test specification for electrical, electronic, and programmable equipment and systems.
IEC 60945 Ed 3	Maritime navigation and radiocommunication equipment and systems – General requirements – Methods of testing and required test results.
IEC 61000-4-2:2008	Electromagnetic compatibility (EMC) - Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test.
IEC 61000-4-3:2020	Electromagnetic compatibility (EMC) - Part 4-3: Testing and measurement techniques - Radiated, radiofrequency, electromagnetic field immunity test.

Standard	Description
IEC 61000-4-4:2012	Electromagnetic compatibility (EMC) - Part 4-4: Testing and measurement techniques - Electrical fast transient/burst immunity test.
IEC 61000-4-5:2014	Electromagnetic compatibility (EMC) - Part 4-5: Testing and measurement techniques - Surge immunity test.
IEC 61000-4-6:2013	Electromagnetic compatibility (EMC) - Part 4-6: Testing and measurement techniques - Immunity to conducted disturbances, induced by radio-frequency fields.
CISPR 16-2-1:2014	Specification for radio disturbance and immunity measuring apparatus and methods - Part 2-1: Methods of measurement of disturbances and immunity - Conducted disturbance measurements.
CISPR 16-2-2:2010	Specification for radio disturbance and immunity measuring apparatus and methods - Part 2-2: Methods of measurement of disturbances and immunity - Measurement of disturbance power.
CISPR 16-2-3:2016	Specification for radio disturbance and immunity measuring apparatus and methods - Part 2-3: Methods of measurement of disturbances and immunity – Radiated disturbance measurement.

6. CONCLUSIONS & NEXT STEPS

6.1 Initial Report Applicability

The SCS was developed to support the complete Current Direct's battery management data acquisition system. To operate the SCSs, a Master Control Unit (MCU) is needed. The prior iteration of this system consisting of a Voltage Balancing Units (VBUs) and BMS Master has been developed and is being deployed as the BattSense technology in industrial applications. In this context, the following EMC tests were performed.

Emission Tests:

- Conducted emissions according to EN55022
- Radiated emissions according to EN55022

Immunity Test:

- Conducted immunity according to IEC 61000-4-6
- Radiated immunity according to IEC 61000-4-3
- Surge test according to IEC 61000-4-5
- Electrical fast transient/Burst test according to IEC 61000-4-4
- Electrostatic Discharge according to IEC 61000-4-2

The above tests are then compared against maritime test standards outlined in DNVGL-CG-0339:

- For the Emissions aspect: The performed emissions tests were in accordance with EN55022 (equivalent to CISPR 22). DNVGL-CG-0339 requires performing emissions tests according to the CISPR 16 standard.
- For the Immunity aspect: The performed tests did not consider conducted low-frequency immunity according to IEC 60945 standard. For the other immunity tests, the tests applied the same requirements covered by the DNVGL standards.

As previously explained, the conditions and test levels on the prior test conducted are not representative of real maritime operational environments. A new EMC test for both the components and complete system should be developed with more demanding test levels and an extended frequency band to ensure compatibility within this operating environment.

6.2 EMC TEST TIMELINE

Due to shortages in the global market (see before) and re-design efforts, the project hasn't been able to provide, in time, a sufficient amount of hardware to support the targeted full-scale demonstrator, nor a representative scaled down version that could be subjected to the planned EMC testing approach.

To comply with the Current Direct project and maritime application requirements in general, the current VITO BMS technology based on a BMS Master and cell connected VBUs needs a hardware redesign to a new MCU + SCS combination as explained in section 3.

This will influence the EMC performance of this BMS subsystem. Two main steps in this redesign process have been finished

1) finalization of the new hardware design;
2) approved functionality on the revised hardware

Only in Q4 2022 both steps were completed. By that time however, no relevant hardware set-up nor budget was available to perform the EMC testing. Hence, the final EMC performance of the BMS component could not be assessed per the project EMC test plan based on international standards and operational environment conditions.